Texas Instruments

ADS5517/25/27/45/46/47 EVM User Guide

User's Guide

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1 Overview

This manual assists users in using the ADS5517/25/27/45/46/47 evaluation module (EVM) for evaluating the performance of the ADS5517/25/27/45/46/47 (ADCs). The EVM provides a powerful and robust capability in evaluation of the many features of the ADCs and the performance of the device under many conditions.

1.1 EVM Basic Functions

Analog input to the ADC is provided via external SMA connectors. The user supplies a single-ended input, which is converted into a differential signal. One input path uses a differential amplifier, while the other input is transformer-coupled.

The EVM provides an external SMA connector for input of the ADC clock. The single-ended input is converted into a differential signal at the input of the device.

Digital output from the EVM is via a 40-pin connector.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the ADC analog and digital supplies, the FPGA supply, and the differential amplifier supply.

CAUTION

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

2 EVM Quick Start Guide

The ADC has two basic modes of output operation, ensuring compatibility in a broad range of systems. Follow the steps below to get the EVM operating quickly with the ADC in either DDR LVDS output mode or CMOS output mode.

Note: Follow the steps in the listed order; not doing so could result in improper operation.

2.1 EVM LVDS Output Mode Quick Start (Default)

1. Ensure a jumper is installed between pins 1 and 2 on JP2.
2. Ensure DIP switch SW1, switch 2 is set to LVDS.
3. Ensure DIP switch SW1, switch 8 is set to PARALLEL.
4. Use a regulated power supply to provide 3.3 VDC to the ADC at J11 and J15, with the corresponding returns connected to J9 and J16.
5. Use a regulated power supply to provide a 5-VDC input to J14, while connecting the return to J17.
6. Provide a filtered, low-phase-noise, sinusoidal 1.5-Vrms, 170-MHz clock to J7.
7. Provide a filtered, sinusoidal analog input to J3.
8. Using a logic analyzer and Table 3 in this manual, monitor the ADC output on J4.

2.2 EVM CMOS Output Mode Quick Start

1. Ensure a jumper is installed between pins 2 and 3 on JP2.
2. Ensure DIP switch SW1, switch 2 is set to CMOS.
3. Ensure DIP switch SW1, switch 8 is set to PARALLEL.
4. Use a regulated power supply to provide 3.3 VDC to the ADC at J11 and J15, with the corresponding returns connected to J9 and J16.
5. Use a regulated power supply to provide a 5-VDC input to J14, while connecting the return to J17.
6. Provide a low-phase-noise, sinusoidal 1.5-Vrms, 170-MHz clock to J7.
7. Provide a filtered sinusoidal analog input to J3.
8. Briefly depress S1, which resets the EVM.
9. Using a logic analyzer and Table 3 in this manual, monitor the ADC output on J4.

3 Circuit Description

3.1 Schematic Diagram

The schematic diagram for the EVM is in Section 5.3 of this document.

3.2 Circuit Function

The following paragraphs describe the function of individual circuits. See the data sheet for complete device operating characteristics.

3.2.1 Configuration Options

The EVM provides a DIP switch, SW1, to control many of the modes of operation when the EVM is configured for parallel-mode operation. Table 1 describes the functionality of the DIP switches.

Note: When the device is configured for serial-mode operation (SW1, switch 8), the DIP settings on SW1, switch 1 through SW1, switch 7 are ignored.

Table 1. DIP Switch SW1

SW1 SWITCH NUMBER	OFF	ON	DESCRIPTION
1	2s complement	Offset binary	Determines device output format
2	LVDS	CMOS	Determines device output mode
3	Reserved	Reserved	Reserved
4	Internal reference	External reference	When set to External Reference, ADC uses common-mode voltage on TP1.
5	Edge = 1	Edge = 2	Allows for output edge programmability
6	Edge = 3	Edge = 4	Allows for output edge programmability
7	Normal	Power down	Allows for power down
8	Serial	Parallel	Determines mode for register interface

By switching SW1, switch 8 to OFF, the ADC operates in serial mode, using its programmed register contents. A complete register map can be found in the device datasheet. Three pins on header J6 have been reserved for programming the device while it operates in serial mode. To program the device registers using header J6, place SCLK on pin 21, SDATA on pin 23, and SEN on pin 25. A pattern generator can be used to generate the patterns needed for programming. Alternatively, TI provides an optional USB daughtercard that plugs into the expansion slot of the EVM. The USB daughtercard allows ADC register control via a software package loaded onto the PC.

3.2.2 Power

Power is supplied to the EVM via banana jack sockets. The EVM offers the capability to supply analog and digital 3.3 V independently to the ADC. Table 2 offers a snapshot of the power-supply options. All supply connections are required for default operation, except J12, J10, J13, and J20.

The EVM provides local decoupling for the ADC; however, the ADC features internal decoupling, and in many cases minimal external decoupling can be used without loss in performance. Users are encouraged to experiment to find the optimal amount of external decoupling required for their application. Figure 1 shows the ADS5547 LVDS-mode performance with all of the decoupling capacitors installed and the performance with C4, C5, C6, C7, C8, C9, and C10 removed. By default, the EVM comes with all of the decoupling capacitors installed.

Table 2. EVM Power Options

BANANA JACK	NAME	VOLTAGE	DESCRIPTION
J9	Device AGND	GND	
J10	AGND	GND	
J11	Device AVDD	3.3	Device analog supply
J12	Amplifier negative rail	–5	THS4509 Vs– supply
J13	Amplifier positive rail	5	THS4509 Vs+ supply
J14	Auxiliary power	5	Supplies power to all peripheral circuitry including the FPGA and PROM. Voltages rails are created by using TI's TPS75003 voltage regulator.
J15	Device DVDD	3.3	Device internal digital output supply
J16	DGND	GND	
J17	DGND	GND	
J20			If TP11, TP12, and TP13 are tied low, the TPS75003 is disabled. In this case, one can supply 3.3 V to pin 1, 1.2 V to pin 2, and 2.2 V to pin 3 of J20 while connecting the ground to J17.

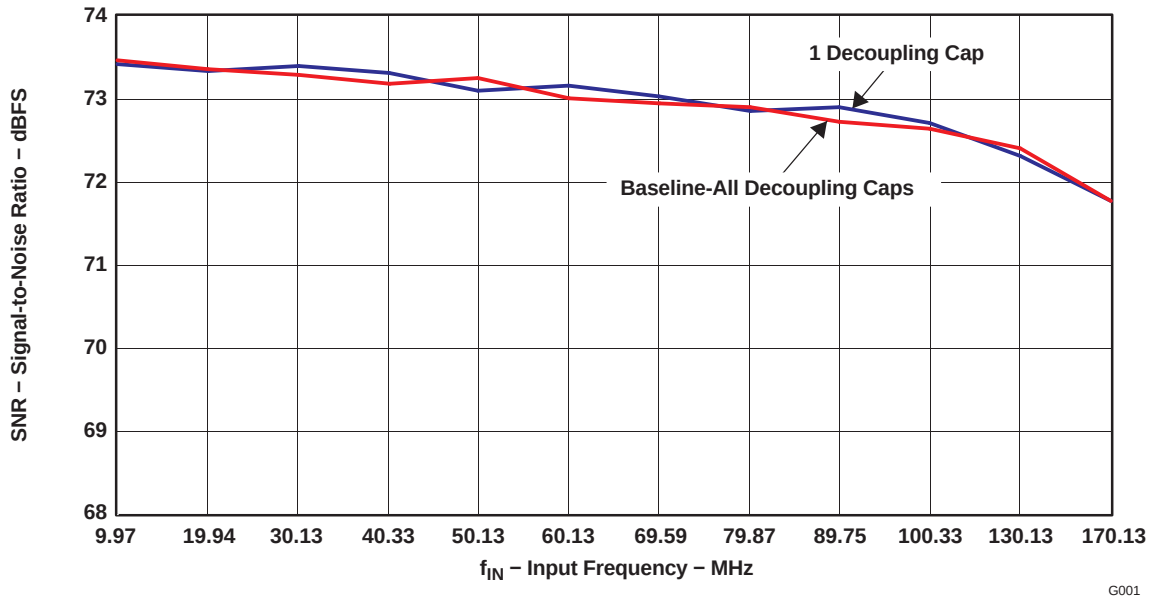

Figure 1. ADS5547 SNR Performance vs Decoupling

3.2.3 Analog Inputs

The EVM can be configured to provide the ADC with either transformer-coupled or differential amplifier inputs from a single-ended source. The inputs are provided via SMA connector J3 for transformer-coupled input or SMA connector J1 for differential amplifier input. To set up for one of these options, the EVM must be configured as follows:

1. For a 1:1 transformer-coupled input to the ADC, a single-ended source is connected to J3. Confirm that SJP4 has pins 2 and 3 shorted, and that SJP5 has pins 2 and 3 shorted. The transformer used, the Mini-Circuits TC4-1W, forms an inherent band-pass filter with a pass band from 3 MHz to 800 MHz. This is the default configuration for the EVM.
2. One can use a TI THS4509 amplifier to drive the ADC by applying an input to J1. Reconfigure SJP4 and SJP5 such that both have pins 1 and 2 shorted. A 5-VDC supply must be connected to the board to provide power to U3 for this configuration.

   The THS4509 amplifier path converts a single-ended signal presented on J1 into a differential signal.

The schematics present various interface options between the amplifier and the ADC. Depending on the input frequencies of interest, further performance optimization can be had by designing a corresponding filter. In its default configuration, R43, R44, and C119 form a first-order, low-pass filter with a cutoff frequency of 70 MHz. Figure 2 shows the performance of the ADS5545 using the THS4509 path.

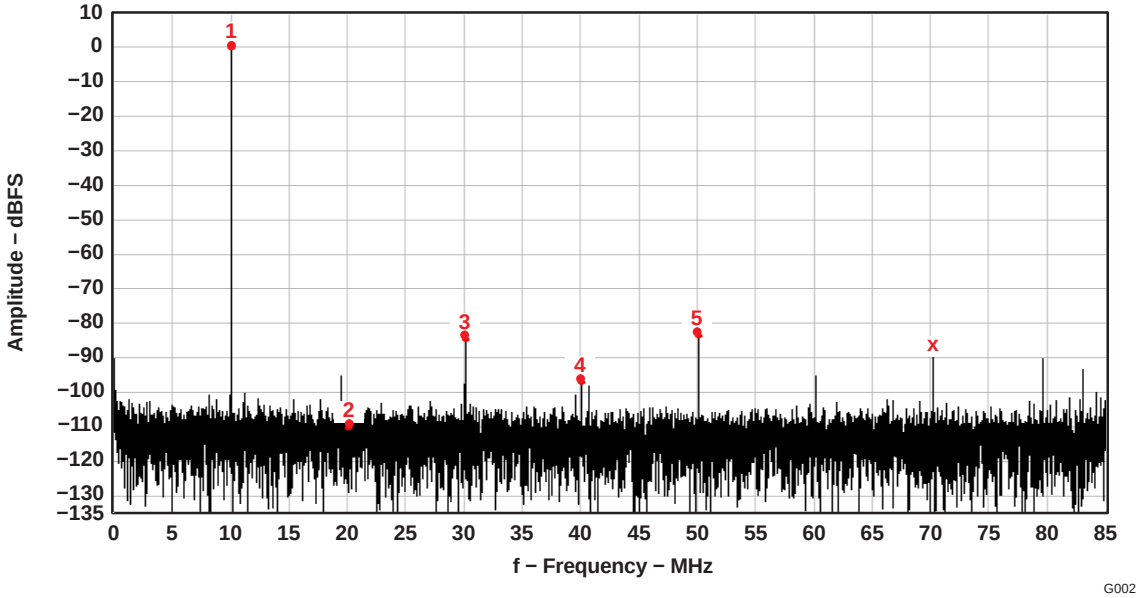

Figure 2. THS4509 + ADS5545 EVM Performance

3.2.4 Clock Input

A single-ended, harmonically filtered, low-phase-noise, 1.5-Vrms sinusoidal input should be applied to J7. The frequency must not exceed the device specification. In the EVM default configuration, both SPJ1 and SJP2 must have pins 1 and 2 shorted.

In the board default configuration, the transformer provides single-ended to differential conversion. The transformer has an impedance ratio of 4.

3.2.5 Digital Outputs

For compatibility with a broad range of logic analyzers, the EVM outputs 3.3-V parallel CMOS data on header J4, independent of the ADC operational mode. The Xilinx™ Spartan™-3E FPGA provides the necessary translation, and it configures itself using one of two different logic files stored in the PROM, based on the EVM configuration. The CMOS data output of the FPGA is contained in data header J4 and is a standard 40-pin header on a 100-mil grid, which allows easy connection to a logic analyzer. The connector pinout is listed in Table 3. For quick setup, the eye diagram is shown in Figure 3. No setup or hold-time adjustments must be made to the logic analyzer if using the rising edge of the output clock to latch in the data.

Note: The eye diagram shown is the output of the FPGA at 210 MSPS, not that of the ADC. For the ADC output timing, see the respective device data sheet.

Table 3. Output Connector J4

J4 PIN	ADS5517 DESCRIPTION	ADS5525/27 DESCRIPTION	ADS5545/46/47 DESCRIPTION
1	CLK	CLK	CLK
2	GND	GND	GND
3	NC	NC	NC
4	GND	GND	GND
5	Reserved	Reserved	Reserved
6	GND	GND	GND
7	Reserved	Reserved	Reserved
8	GND	GND	GND
9	NC	NC	Data bit 0 (LSB)
10	GND	GND	GND
11	NC	NC	Data bit 1
12	GND	GND	GND
13	NC	Data bit 0 (LSB)	Data bit 2
14	GND	GND	GND
15	Data bit 0 (LSB)	Data bit 1	Data bit 3
16	GND	GND	GND
17	Data bit 1	Data bit 2	Data bit 4
18	GND	GND	GND
19	Data bit 2	Data bit 3	Data bit 5
20	GND	GND	GND
21	Data bit 3	Data bit 4	Data bit 6
22	GND	GND	GND
23	Data bit 4	Data bit 5	Data bit 7
24	GND	GND	GND
25	Data bit 5	Data bit 6	Data bit 8
26	GND	GND	GND
27	Data bit 6	Data bit 7	Data bit 9
28	GND	GND	GND
29	Data bit 7	Data bit 8	Data bit 10
30	GND	GND	GND
31	Data bit 8	Data bit 9	Data bit 11
32	GND	GND	GND
33	Data bit 9	Data bit 10	Data bit 12
34	GND	GND	GND
35	Data bit 10 (MSB)	Data bit 11 (MSB)	Data bit 13 (MSB)
36	GND	GND	GND
37	NC	NC	NC
38	GND	GND	GND
39	NC	NC	NC
40	GND	GND	GND

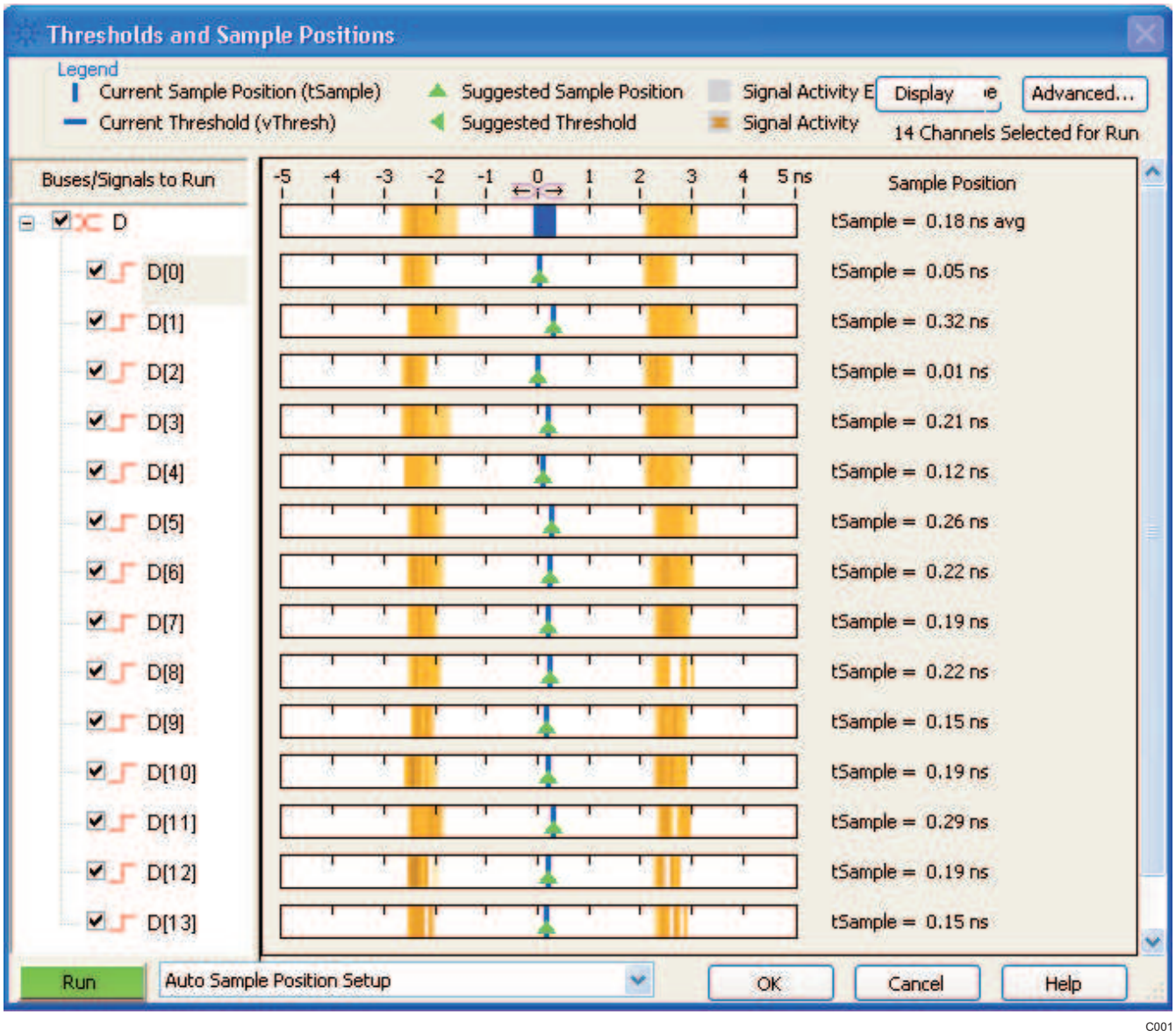

Figure 3. Eye Diagram of Data on Header J4.

3.2.6 Test Points

For added EVM visibility and control, several test points are provided. Table 4 summarizes the test points available.

Table 4. Test Points

TP	DESCRIPTION
TP1	ADC common mode, input or output depending on the setting of SW1, switch 4
TP3	THS4509 power down
TP4	ADC output enable
TP5	AGND
TP6	AGND
TP7	AGND
TP8	DGND
TP9	FPGA M0 pin; determines which FPGA logic file to load
TP10	ADC SCLK
TP11	TPS75003 1.2 enable
TP12	TPS75003 2.5 enable
TP13	TPS75003 3.3 enable

3.2.7 LED Operation

To give greater visibility into the EVM operations, two LEDs are provided, D3 and D4. On power up, D4 is asserted when a successful FPGA boot up is complete. For correct EVM operation, the LED should be asserted at all times. LED D3 is asserted when the ADC and FPGA are operating and decoding in DDR LVDS mode, and is not asserted when the ADC is functioning in CMOS mode. Furthermore, in either DDR LVDS mode or CMOS mode, LED D3 blinks when an ADC over-range condition occurs.

CAUTION

If LED D3 is blinking, the amplitude coming into the ADC input (J3 or J4) must be attenuated immediately; otherwise, damage to the ADC could occur.

4 Expansion Options

The EVM offers several exciting possibilities to expand the capabilities of the EVM. This allows the utmost flexibility when prototyping an ADC circuit under conditions that mimic the end system, without the need to develop a custom prototype board.

4.1 Custom FPGA Code

Using a standard JTAG interface on JP1, users have the ability to load custom logic onto the FPGA, rapidly speeding up digital development time. This allows the flexibility of prototyping and debugging an ADC digital interface design before developing application-specific hardware.

To take advantage of the onboard FPGA, users can download the free Xilinx WebPACK™ from the Xilinx Web site. Select the XC3S250E-4FT256 as the FPGA and the XCF16PFSG48 as the PROM.

Note: See the Xilinx Spartan-3E Web site for complete documentation of the FPGA at: http://direct.xilinx.com/bvdocs/publications/ds312.pdf

Schematically, the FPGA is configured in BPI mode, and it samples FPGA pins M2, M1, and M0 when the FPGA's INIT_B is brought low. Depending of the status of M0, it boots from either the top or the bottom of the PROM contents. The PROM allows for the storage of two FPGA bit files. In its default condition, the EVM stores one file for ADC CMOS output at the beginning of the PROM address space and one file for ADC LVDS output at the end of the PROM address space.

Note: When creating custom FPGA code, store any custom-developed bit files for ADC CMOS operation in the PROM revision 0 space, and store any custom-developed FPGA code for ADC LVDS operation in the PROM revision 1 space.

4.2 Expansion Slot

For those users who make use of a custom FPGA program on the EVM, J5 and J6 provide an expansion-slot capability. Users can design daughtercards or breakout boards to make use of the unused FPGA I/O pins which are brought out to the headers.

Note: The EVM provides 5 V from J14 to pin 1 of both J5 and J6. This can be used to provide power to any designed daughtercards.

4.3 Optional USB SPI Interface

In most cases, users can use the ADC parallel interface mode to change the operational modes of the ADC. For users requiring SPI control of the ADC, TI has developed an optional USB daughter card that plugs into the expansion slot. With the USB daughter card, users can use a PC interface to communicate to the ADC three-wire SPI interface, which allows for complete control of the ADC register map. Contact the factory for this optional accessory.

5 Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM.

5.1 PCB Layout

The EVM is constructed on a 6-layer, 0.062-inch thick PCB using FR-4 material. The individual layers are shown in Figure 4 through Figure 9. The layout features split analog and digital ground planes; however, similar performance can be had with careful layout using a single ground plane. Users can connect the analog and digital ground planes underneath the EVM by soldering the two exposed tinned strips together.

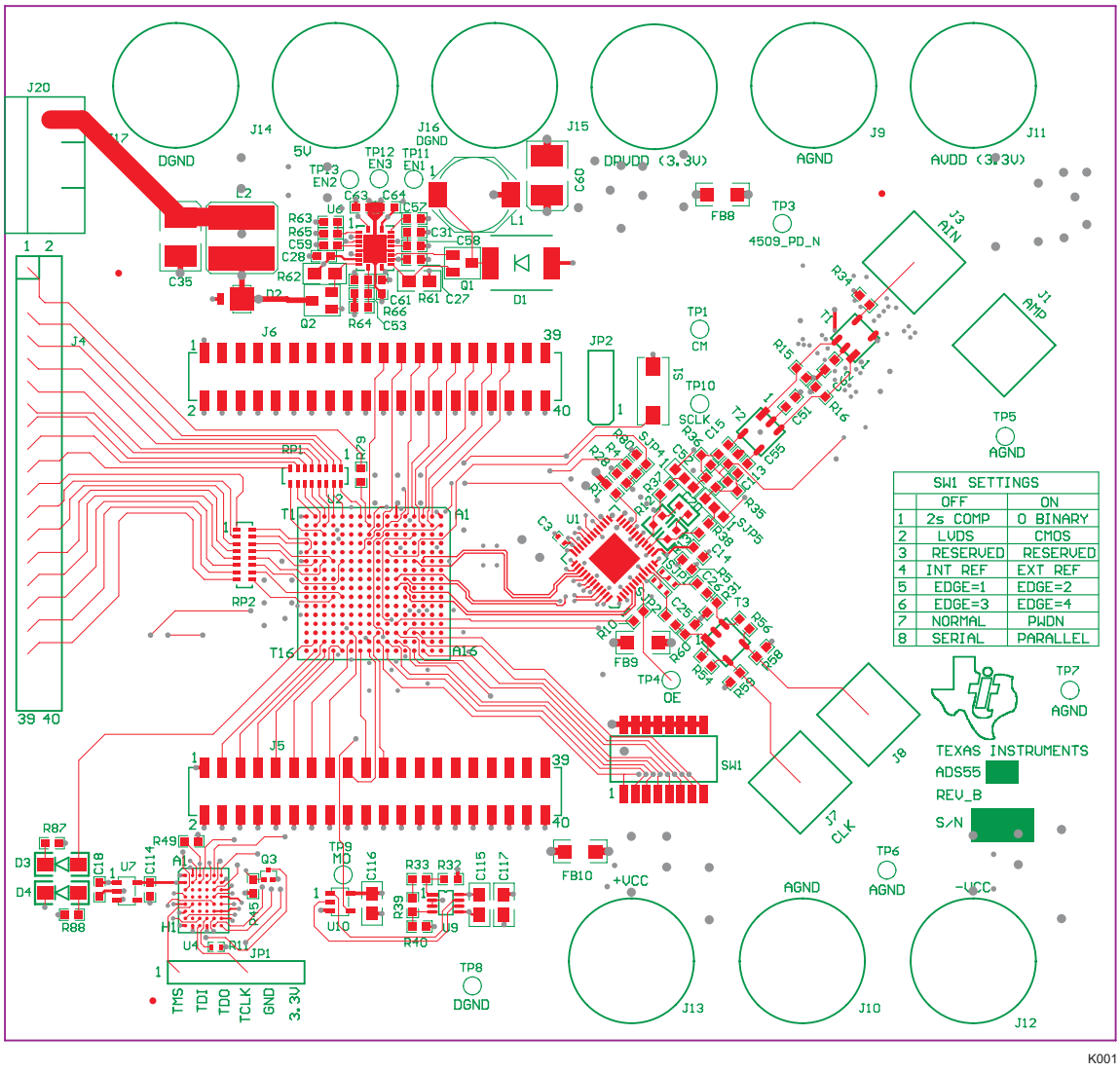

Figure 4. Top Layer

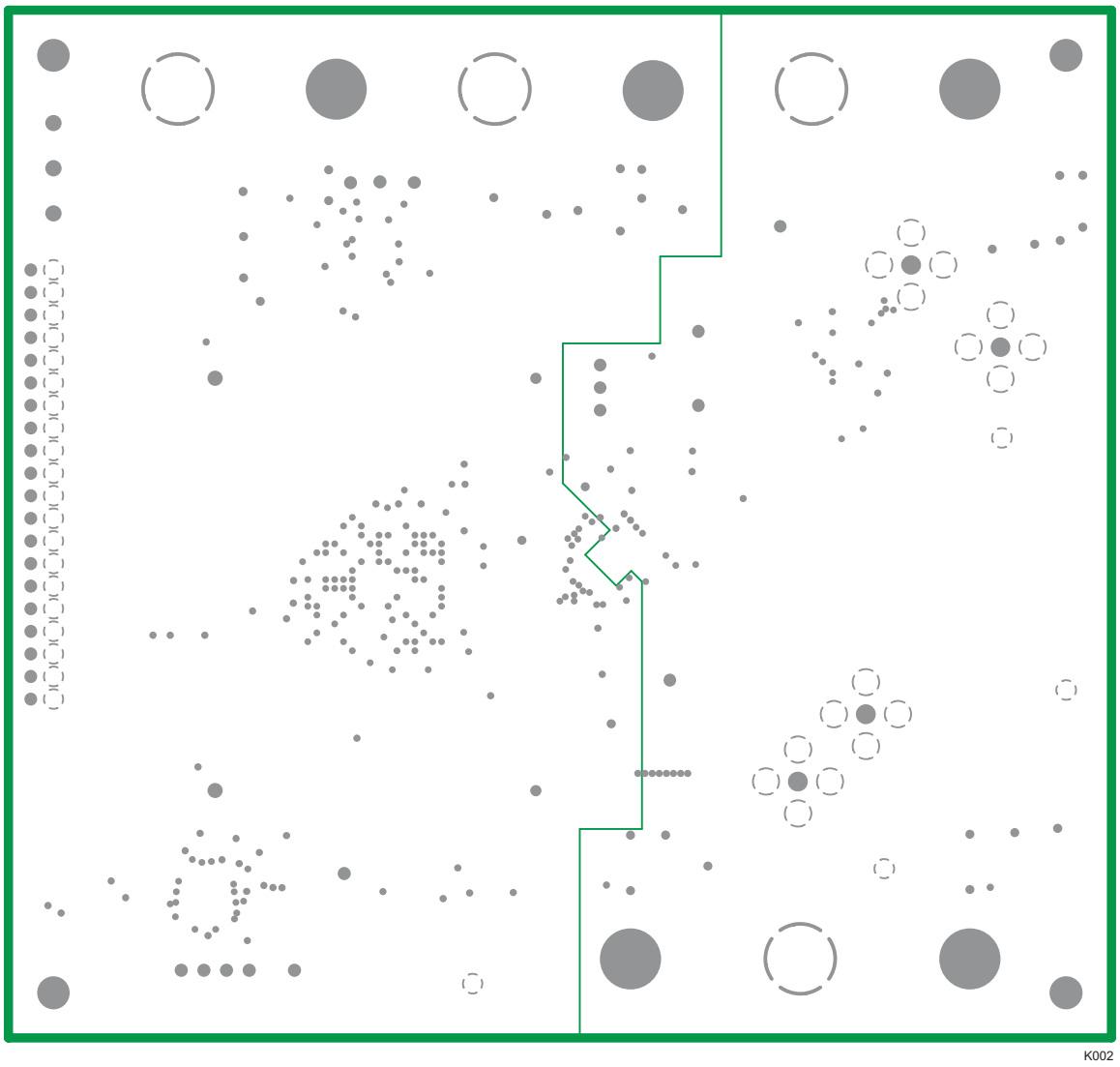

Figure 5. Layer 2, Ground Plane

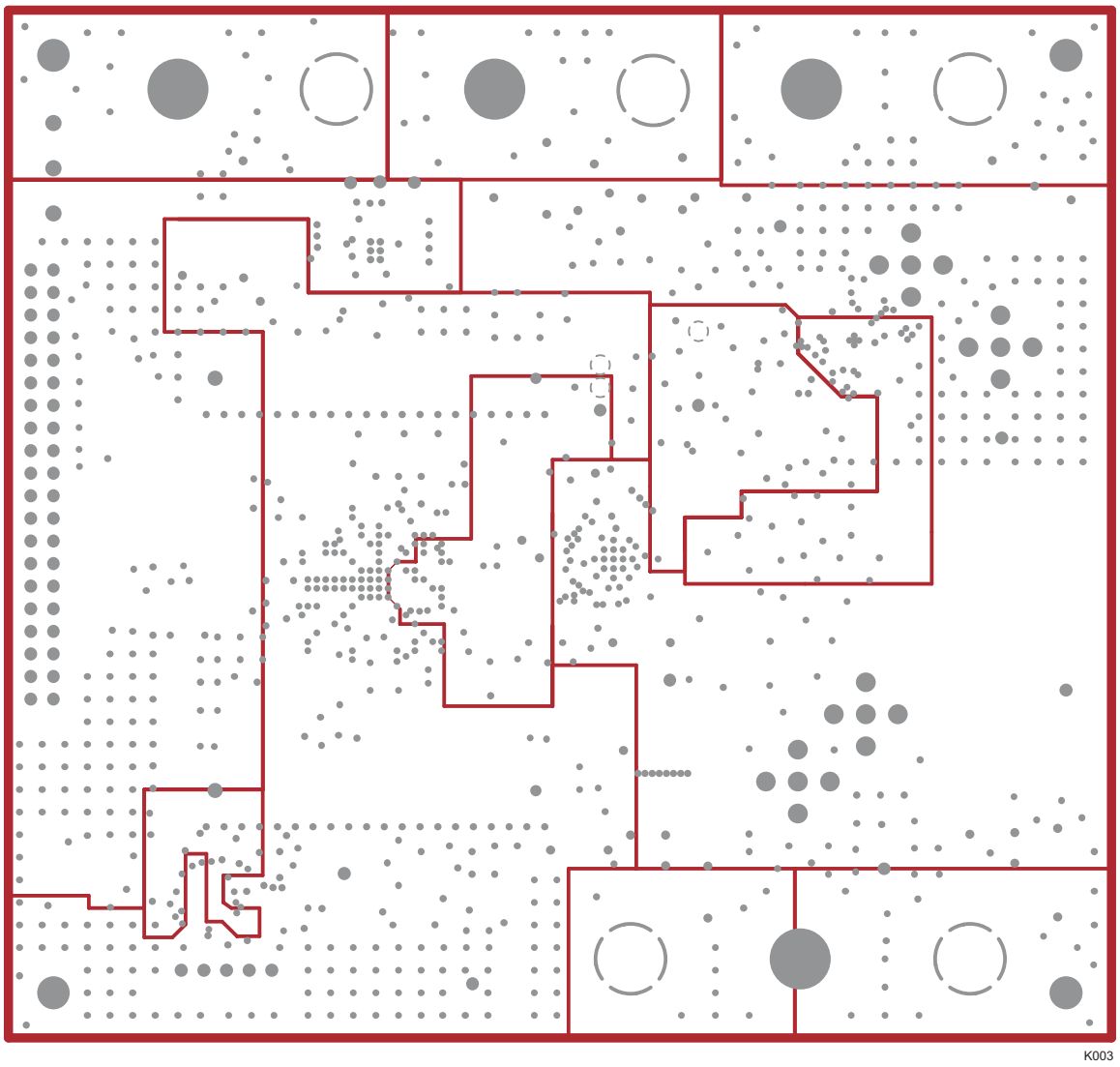

Figure 6. Layer 3, Power Plane #1

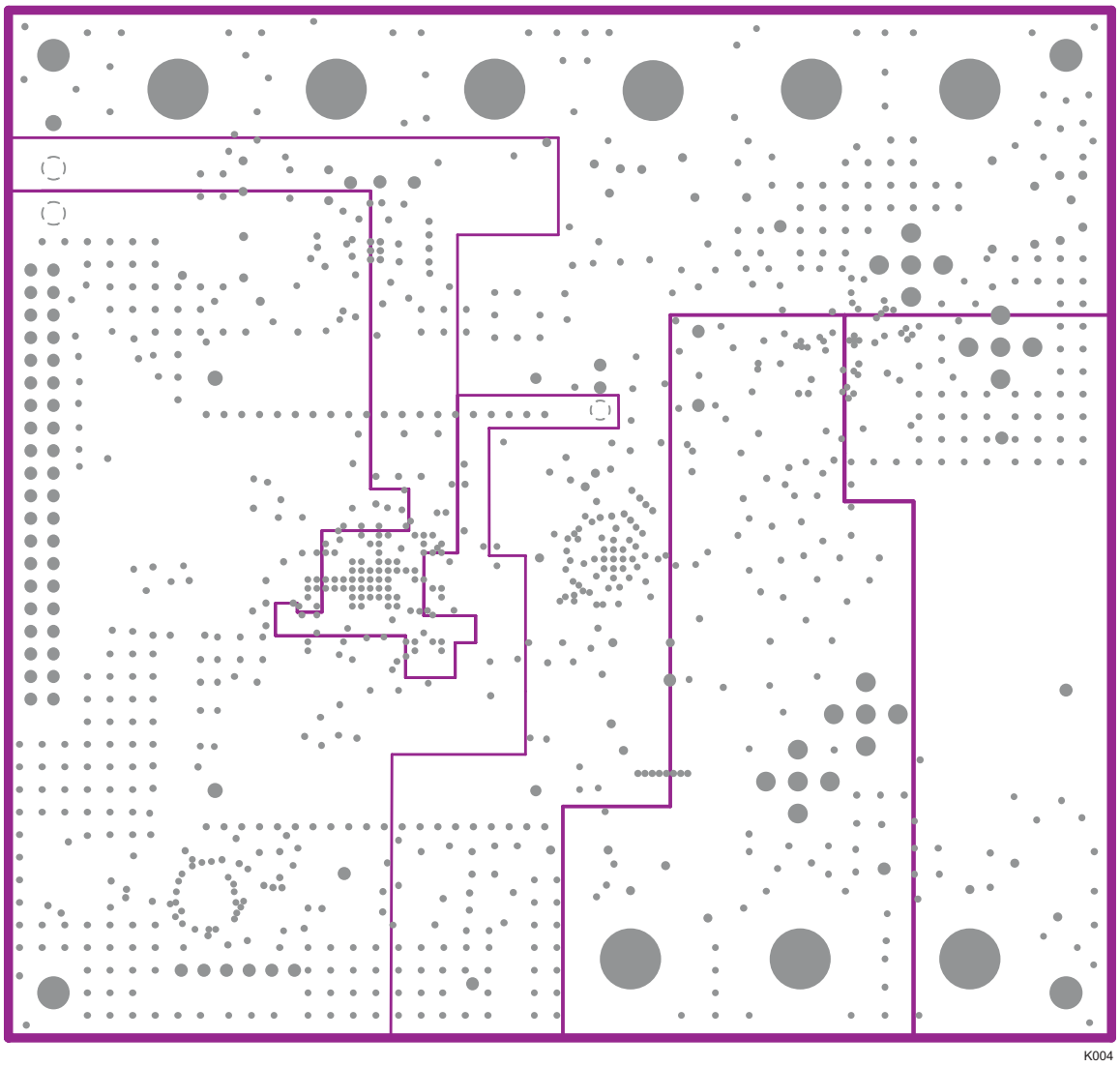

Figure 7. Layer 4, Power Plane #2

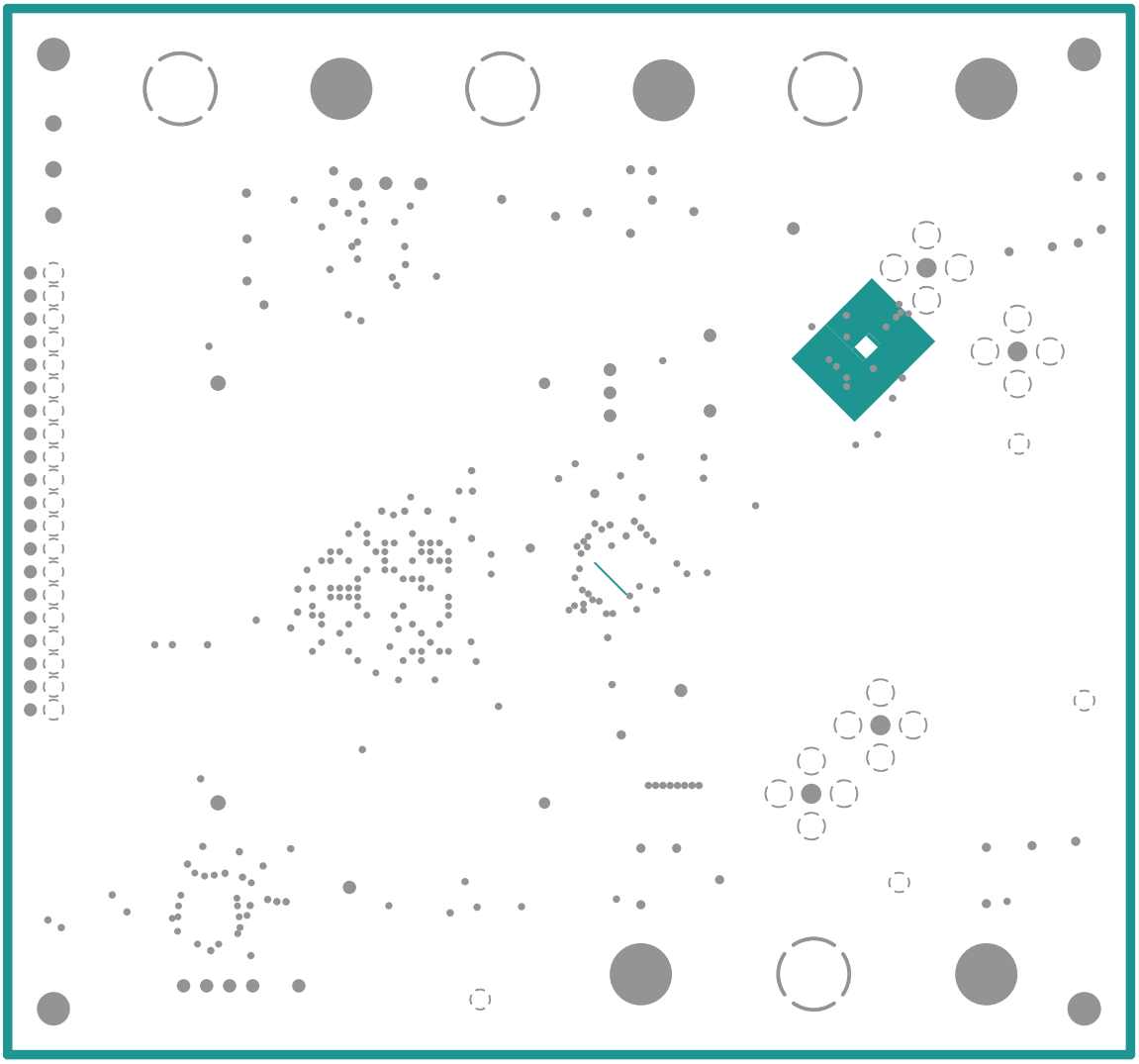

Figure 8. Layer 5, Ground Plane

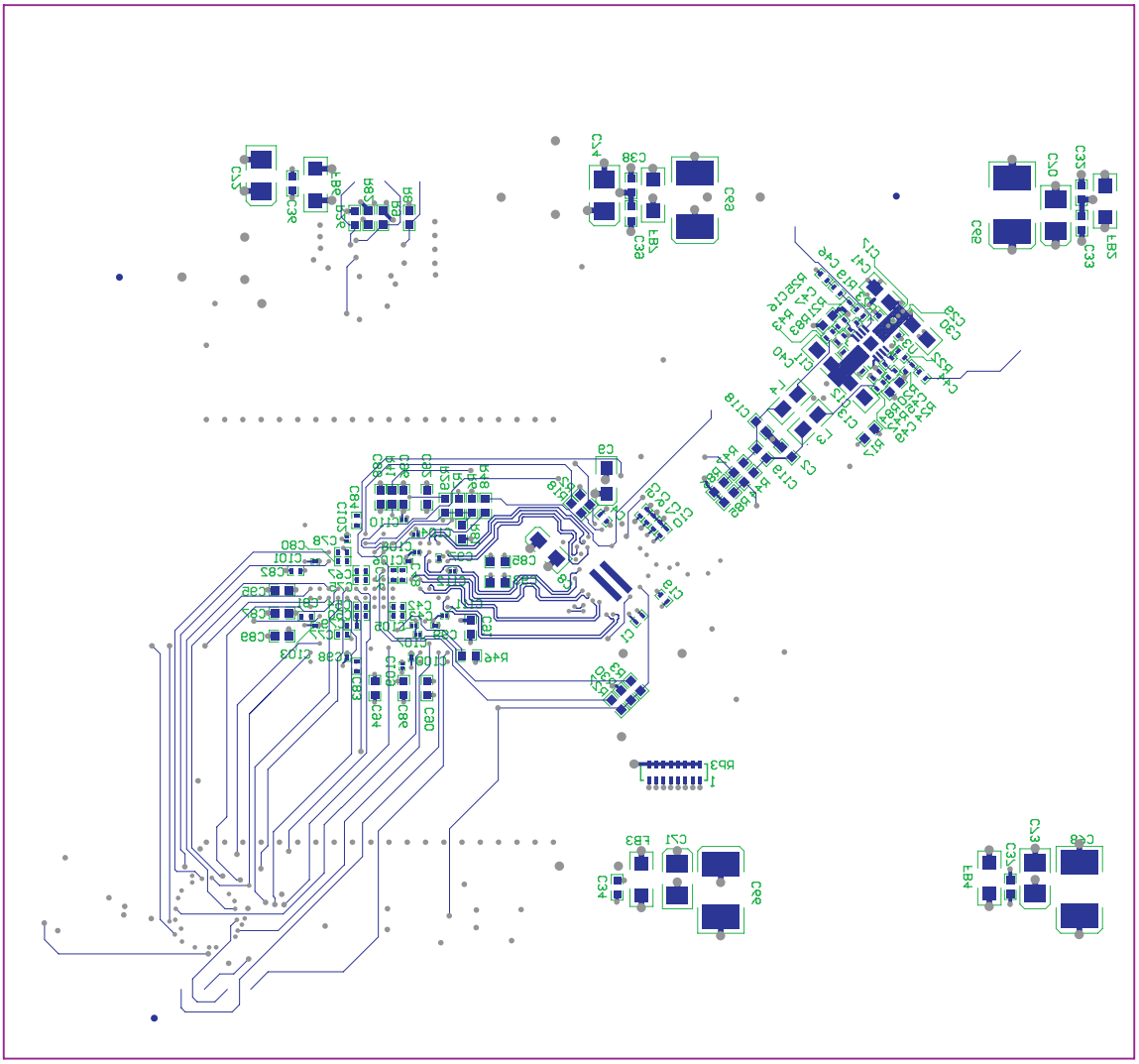

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Figure 9. Layer 6, Bottom Layer

5.2 Bill of Materials

The bill of materials appears on the following page.

Table 5. Bill of Materials

VALUE	FOOTPRINT	QTY	PART NUMBER	VENDOR	DIGI-KEY NUMBER	REF DESIGNATOR	NOT INSTALLED
CAPACITORS							
47-µF, tantalum, 20%, 10-V	7343	4	ECS-T1AD476R	Panasonic	PCS2476CT-ND	C65, C66, C68, C69	
10-µF, 10-V, 20%	3528	5	ECS-T1AX106R	Panasonic	PCS2106CT-ND	C70, C71, C72, C73, C74	
10-µF, 10-V, 20%	3216	2	ECS-T1AY106R	Panasonic	P11309CT-ND	C8, C9	
100-µF, 6.3-V, 10%	6032	2	TPSC107K006R0150	AVX	478-1764-2-ND	C35, C60	
0.1-µF, 16-V, 10%	805	2	ECJ-2VB1C104K	Panasonic	PCC1812CT-ND	C115, C116	
2.2-µF, 6.3-V, 10%	805	1	ECJ-GVB0J225K	Panasonic	PCC2310CT-ND	C117	
10-µF, 6.3-V, 10%	805	4	GRM21BR60J106KE19L	Murata	490-1717-1-ND	C13, C30, C40, C41	
0.01-µF, 16-V, 10%	603	1	ECJ-1VB1C103K	Panasonic	PCC1750CT-ND	C57	
0.1-µF, 16-V, 10%	603	18	ECJ-1VB1C104K	Panasonic	PCC1762CT-ND	C14, C15, C18, C25, C26, C27, C28, C32, C33, C34, C36, C37, C38, C39, C51, C55, C62, C113	C52
1.5-nF, 50-V, 10%	603	3	C1608X7R1H152K	TDX		C31, C58, C59	
10-pF, 50-V, ±0.5-pF	603	1	ECJ-1VC1H100D	Panasonic	PCC100CVCT-ND	C53	
1-µF, 6.3-V, 10%	603	1	ECJ-1VB0J105K	Panasonic	PCC1915CT-ND	C64	
10-µF, 6.3-V, 20%	603	1	ECJ-1VB0J106M	Panasonic	PCC2395CT-ND	C63	
100-µF, 4-V, 20%	603	1	NOJC107M004RWJ	AVX	478-1824-1-ND	C61	
2.2-µF, 6.3-V, 10%	603	13	ECJ-1VB0J225K	Panasonic	PCC2273CT-ND	C85–C96, C114	
18-pF, 50-V, 5%	603	1	GRM1885C1H180JA01D	Murata	490-1409-1-ND	C119	C2, C118
2-pF, 100-V, ±0.25-pF	603	0	GQM1885C2A2R0CB01D	Murata	490-3555-1-ND		C20
0.1-µF, 16-V, +80/–20%	402	14	ECJ-0EF1C104Z	Panasonic	PCC1731CT-ND	C1, C3, C4, C5, C6, C7, C10, C11, C12, C16, C17, C19, C29, C44, C49	
0.22-µF, 6.3-V , ±10%	402	17	ECJ-0EB0J224K	Panasonic	PCC2269CT-ND	C42, C43, C46, C48, C50, C54, C67, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84	
0.022-µF, 6.3-V, +80/–20%	201	16	02016G223ZAT2A	AVX	478-1054-1-ND	C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112	

Table 5. Bill of Materials (continued)

VALUE	FOOTPRINT	QTY	PART NUMBER	VENDOR	DIGI-KEY NUMBER	REF DESIGNATOR	NOT INSTALLED
RESISTORS							
0-Ω, 1/10-W, 5%	603	7	ERJ-3GEY0R00V	Panasonic	P0.0GCT-ND	R5, R6, R10, R18, R48, R58, R82	R54, R56
0-Ω, 1/10-W, 5%	402	3	ERJ-GE0R00X	Panasonic	P0.0JCT-ND	R11, C45, C47	
4.02-Ω, 1/10-W 1%	603	2	9C06031A4R02FGHFT	Yageo	311-4.02HCT-ND	R37, R38	
20-Ω, 1/16-W, 1%	603	1	ERJ-3EKF20R0V	Panasonic	P20.0HCT-ND	R79	
24.9-Ω, 1/16-W, 1%	603	1	ERJ-3EKF24R9V	Panasonic	P24.9HCT-ND	R17	
4.7-Ω, 1/2-W, 5%	603	2	ERD-S1TJ4R7V	Panasonic	P4.7BBCT-ND	R44, R47	
36-Ω, 1/10-W, 1%	603	0	RC0603FR-0736RL	Yaego	311-36.0HRCT-ND		R12, R13
49.9-Ω, 1/16-W, 1%	603	2	ERJ-3EKF49R9V	Panasonic	P49.9HCT-ND	R35, R36	R34, R59
100-Ω, 1/16-W, 0.1%	603	3	ERA-3YEB100V	Panasonic	P100YCT-ND	R31, R41, R60	
200-Ω, 1/16-W, 1%	603	2	ERJ-3EKF2000V	Panasonic	P200HCT-ND	R15, R16	R85, R86
330-Ω, 1/16-W, 5%	603	3	ERA-V33J331V	Panasonic	P330CHCT-ND	R45, R87, R88	
499-Ω, 1/16-W, 1%	603	2	ERJ-3EKF4990V	Panasonic	P499HCT-ND	R83, R84	
10-kΩ, 1/16-W, 1%	603	11	ERJ-3EKF1002V	Panasonic	P10.0KHCT-ND	R2, R3, R4, R7, R8, R9, R26, R32, R33, R39, R40	
4.75-kΩ, 1/16-W, 1%	603	2	ERJ-3EKF4751V	Panasonic	P4.75KHCT-ND	R46, R49	
15.4-kΩ, 1/16-W, 1%	603	1	ERJ-3EKF1542V	Panasonic	P15.4KHCT-ND	R65	
20-kΩ, 1/16-W, 1%	603	3	ERJ-3EKF2002V	Panasonic	P20.0KHCT-ND	R30, R80, R81	
36.5-kΩ, 1/16-W, 1%	603	1	ERJ-3EKF3652V	Panasonic	P36.5KHCT-ND	R66	
56.2-kΩ, 1/16-W, 1%	603	1	ERJ-3EKF5622V	Panasonic	P56.2KHCT-ND	R1	
4.99-kΩ, 1/16-W, 1%	603	3	ERJ-3EKF4991V	Panasonic	P4.99KHCT-ND	R27, R28, R29	
61.9-kΩ, 1/16-W, 1%	603	2	ERJ-3EKF6192V	Panasonic	P61.9KHCT-ND	R63, R64	
0.033-Ω, 1/4-W, 5%	805	2	RL1220T-R033-J	Susumu Co,. Ltd.	RL12T.033JCT-ND	R61, R62	
348-Ω, 1/16-W, 1%	402	2	ERJ-2RKF3480X	Panasonic	P348LCT-ND	R24, R25	
49.9-Ω, 1/16-W, 1%	402	3	ERJ-2RKF49R9X	Panasonic	P49.9LCT-ND	R19, R42, R43	
78.7-Ω, 1/16-W, 1%	402	2	ERJ-2RKF78R7X	Panasonic	P78.7LCT-ND	R20, R21	
100-Ω, 1/16-W, 1%	402	2	ERJ-2RKF1000X	Panasonic	P100LCT-ND	R22, R23	
20-Ω R-pack, 5%, 0.063-W	CTS-742_8RES	2	742C163220JTR	CTS	742C163220JCT-ND	RP1, RP2	
10-kΩ resistor pack	CTS_742_8RES	1	742C163103JTR	CTS	742C163103JCT-ND	RP3	

Table 5. Bill of Materials (continued)

VALUE	FOOTPRINT	QTY	PART NUMBER	VENDOR	DIGI-KEY NUMBER	REF DESIGNATOR	NOT INSTALLED
FERRITE BEADS, CONNECTORS, JUMPERS, JACKS, ICs, ETC.							
Ferrite bead	1206	5	EXC-ML32A680U	Panasonic	P10437CT-ND	FB2, FB3, FB4, FB6, FB7	FB8, FB9, FB10
Inductor, SMT, 15-µH, 2.6-A	COIL-CDRH8D43	1	CDRH8D43-150	Sumida		L1	
Inductor, SMT, 5-µH, 2.9-A	COIL-CDRH6D38	1	CDRH6D38-5R0	Sumida	CDRH6D38-5R0NC-ND	L2	
0.0-Ω, 1/8-W, 5% resistor	805	2	ERJ-6GEY0R00V	Panasonic	P0.0ACT-ND	L3, L4	
Red test point	Test_point2	8	5000k	Keystone	5000K-ND	TP1, TP4, TP9, TP10	TP3 TP11 TP12 TP13
Black test point	Test_point2	4	5001k	Keystone	5000K-ND	TP5 TP6 TP7 TP8	
40-pin header	20×2×.1	1	HTSW-120-07-L-D	Samtec		J4	
40-pin header smt	20X2_SMT_MMS_SAMTEC	2	MMS-120-02-T-DV	Samtec		J5, J6	
Red banana jacks	BANANA_JACK	5	ST-351A	Allied	N/A	J11, J12, J13, J14, J15	
Black banana jacks	BANANA_JACK	4	ST-351B	Allied	N/A	J9, J10, J16, J17	
SMA connectors	SMA_Jack	3	901-144-8RFX	AMP	ARFX1231-ND	J1, J3, J7	J8
3POS_header	3pos_jumper	1	HTSW-150-07-L-S	Samtec		JP2(1)	
6-pin header	6×1×.1	1	HTSW-120-07-L-D	Samtec		JP1	
3-pin power connector	3term_screw_con	0	93F7124	Newark			J20
Transformer	TC4-1W_TRANSFORMER	3	TC4-1W	Mini-Circuits		T1, T2, T3	
Diode, Schottky, 1-A, 20-V	DIODE-MBRM120	1	MBRM120E	ON Semiconductor		D2	
Diode, Schottky, 3-A, 20-V	DO-214AB(SMC)	1	SS32	Vishay		D1	
Green SM_LED_1206	LED-1206	2	CMD15-21VGC/TR8	Panasonic	L62205CT-ND	D3, D4	
MOSFET, P-CH, 20-V, 4.7-A, 39-MΩ	3-SOT-23	2	SI2323DS	Vishay		Q1, Q2	
TRANS BIAS NPN, 50-V	SOT416	1	DTC114EET1	ON Semiconductor	DTC114EET1OS-ND	Q3	
Switch	EVQ-PJ	1	EVQ-PJX04M	Panasonic	P8050SCT-ND	S1	
Switch, 8-Pos, half-pitch SMT	SWITCH_8POS_SMT	1	TDA08H0SK1	ITT	CKN1365-ND	SW1	
3-circuit jumpers	SJP3_RESISTOR	2	ERJ-3GEY0R00V	Panasonic	P0.0GCT-ND	SJP4(2), SJP5(3)	
3-circuit jumpers	SJP3_402	2	ERJ-2GE0R00X	Panasonic	P0.0JCT-ND	SJP1(4), SJP2(5)	

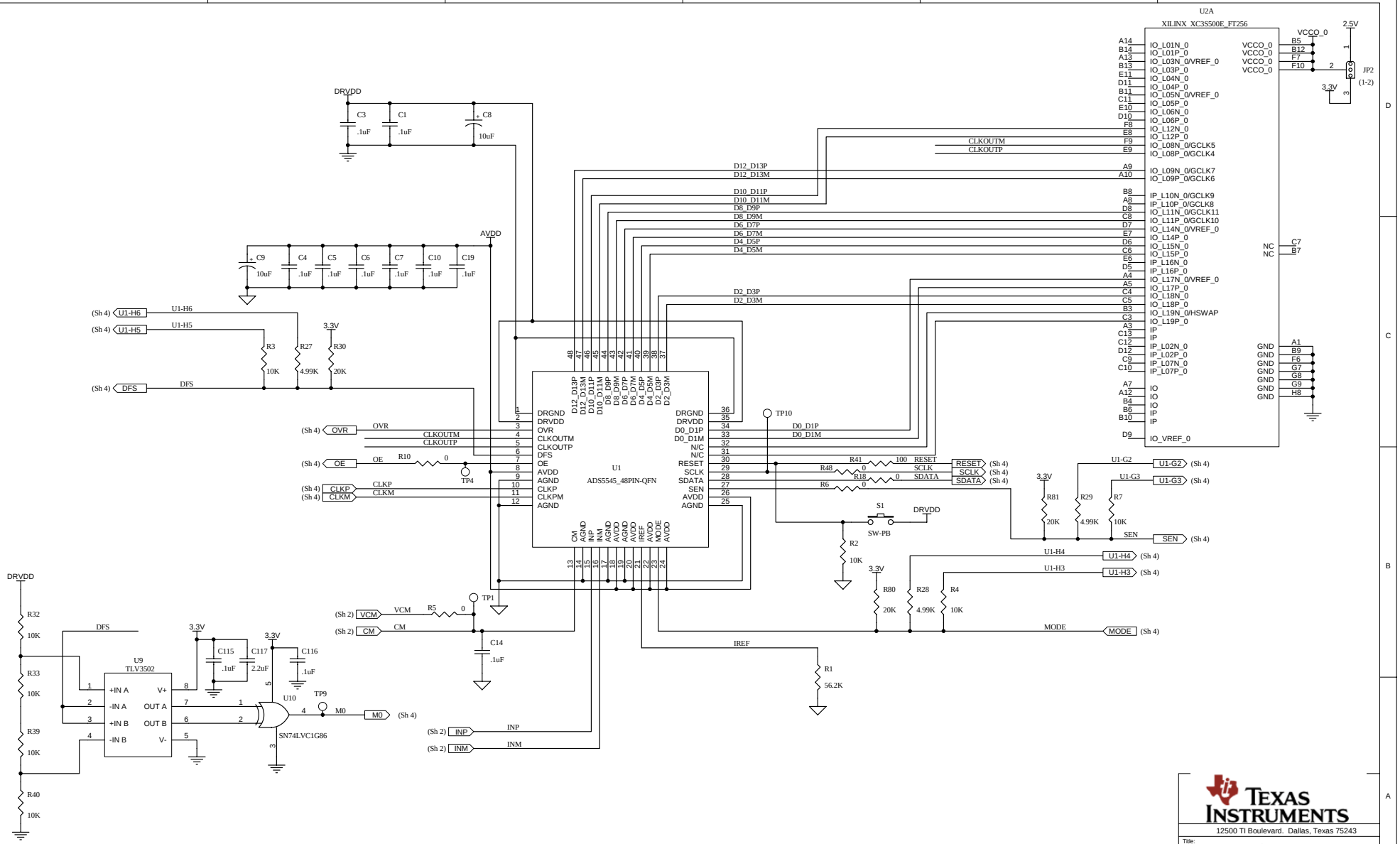
(1) Add jumper for JP2 between pins 1 to 2.
(2) Add jumper for SJP4 between pins 2 and 3 (use a 0-Ω resistor to short pins).
(3) Add jumper for SJP5 between pins 2 and 3 (use a 0-Ω resistor to short pins).
(4) Add jumper for SJP1 between pins 1 and 2 (use a 0-Ω resistor to short pins).
(5) Add jumper for SJP2 between pins 1 and 2 (use a 0-Ω resistor to short pins).

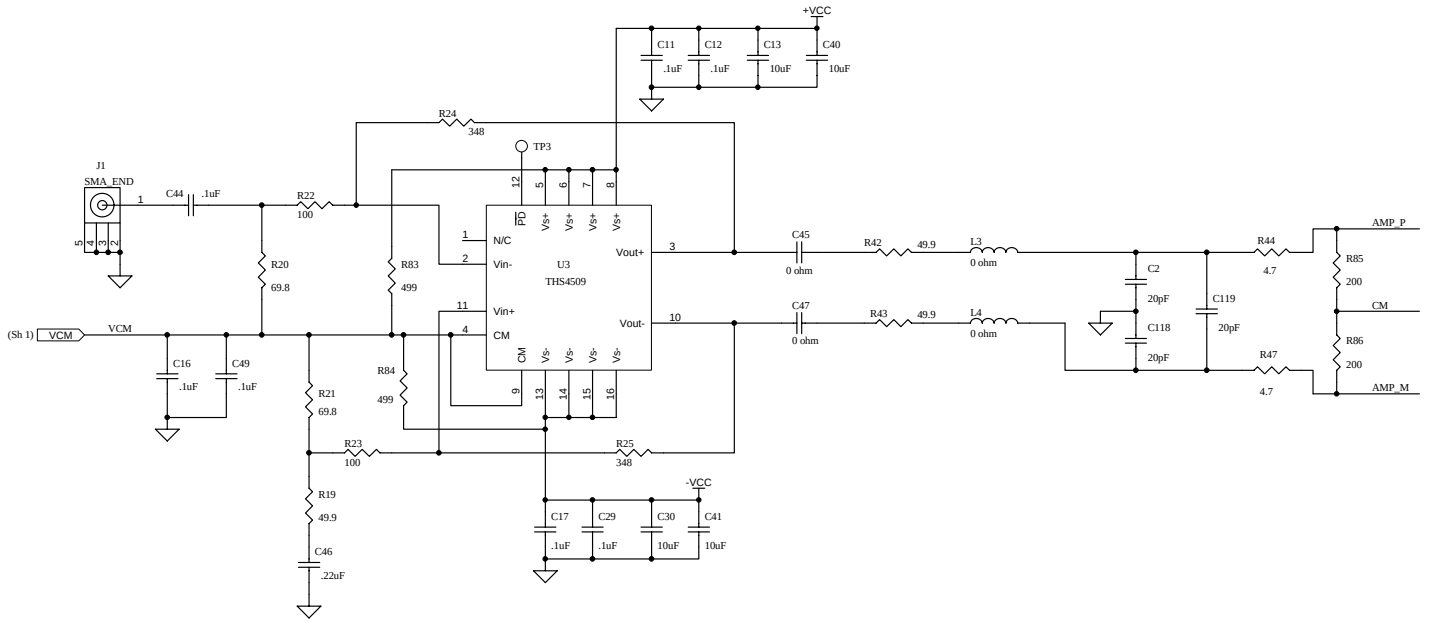
Table 5. Bill of Materials (continued)

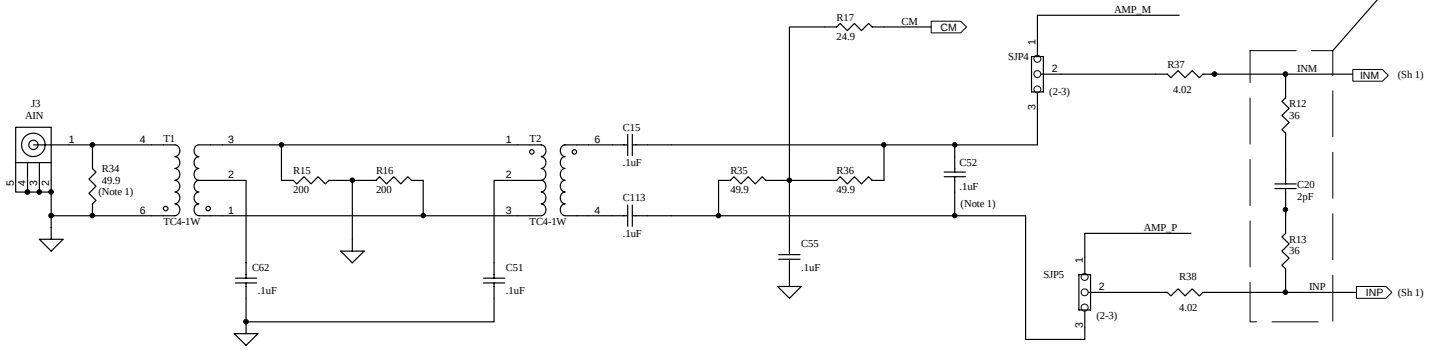
VALUE	FOOTPRINT	QTY	PART NUMBER	VENDOR	DIGI-KEY NUMBER	REF DESIGNATOR	NOT INSTALLED
ADS5517/25/27, ADS5545/46/47	48-QFN_MOD	1	ADS5517/25/27, ADS5545/46/47	TI		U1	
Spartan-3E XC3S250E	256-BGA-1mm_XILINX		XC3S250E-4FT256CES	Xilinx		U2	
IC amp, fully-diff, wideband	16-QFN(RGT)	1	THS4509RGTT	TI	296-17730-1-ND	U3	
XCF16PFSG48	48PIN_BGA_XILINX	1	XCF16PFSG48	Xilinx		U4	
IC, pwr-mgmt, triple-supply	20-pin-QFN	1	TPS75003RHLR	TI	296-17835-2-ND	U6	
IC, LDO reg, hi-PSRR, 1.8-V	5-SOT(DBV)	1	TPS73018DBVT	TI	296-17577-1-ND	U7	
IC, comparator, R-R, hi-spd	8-TSSOP(DCN)	1	TLV3502AIDCNT	TI	296-18147-2-ND	U9	
IC, EX-OR gate, 2-in	5-SOT(DBV)	1	SN74LVC1G86DBVR	TI	296-9853-1-ND	U10	
2-pos shunt	Shorting jumper	1	N/A	3M	929955-06-ND		
Screw	4-40 × 3/8"	4	N/A	Building Fasteners	H781-ND		
Standoff, hex (1/4 x .5")	4-40 screw	4	N/A	Keystone	1902CK-ND		

5.3 PCB Schematics

The schematics for the EVM are on the following pages.


U2A
XILINX_XC3S500E_FT256
U1
ADS5545_48PIN-QFN
U9
TLV3502
U10
SN74LVC1G86
DRVDD
AVDD
3.3V
2.5V
VCCO_0
JP2
(1-2)
SW-PB
TP1
TP4
TP9
TP10
IREF
VCM
CM
INP
INM
MODE
OVR
CLKOUTM
CLKOUTP
CLKP
CLKM
OE
DFS
SEN
SCLK
SDATA
RESET
M0
D12_D13P
D12_D13M
D10_D11P
D10_D11M
D8_D9P
D8_D9M
D6_D7P
D6_D7M
D4_D5P
D4_D5M
D2_D3P
D2_D3M
D0_D1P
D0_D1M
Note 1. Part not installed
Texas Instruments
12500 TI Boulevard. Dallas, Texas 75243
Title: ADS5545
Engineer: J. VENABLE
Drawn By: Y. DEWONCK
FILE:
SIZE:
DATE: 11-Jul-2006
REV: B
SHEET: 1 OF: 7





AMPLIFIER PATH:

AC Couple (default)

C45 C47 = 0.1uF
R26 R27 = 200 Ohms
R5 = 0 Ohms
VCC= 5 V, VEE = GND

DC Couple

C45 C47 = 0 Ohms
R26 R27 = Unpopulated
R5 = Unpopulated
VCC= 4 V, VEE = -1V

Note : R12, C20, and R13 are to be un-populated on ADS5525/45/46 EVMs.

R12, C20, and R13 may be populated for future ADC boards; contact factory for details.

Note 1. Part not installed

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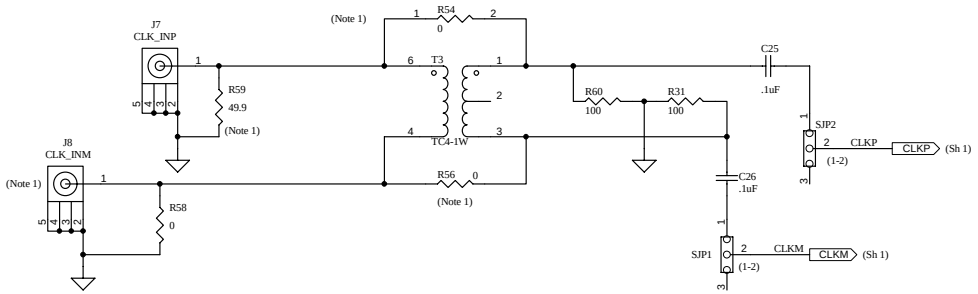
SHEET: 2 OF: 7	



Note 1. Part not installed

Engineer:	J. VENABLE
Drawn By:	Y. DEWONCK
FILE:	

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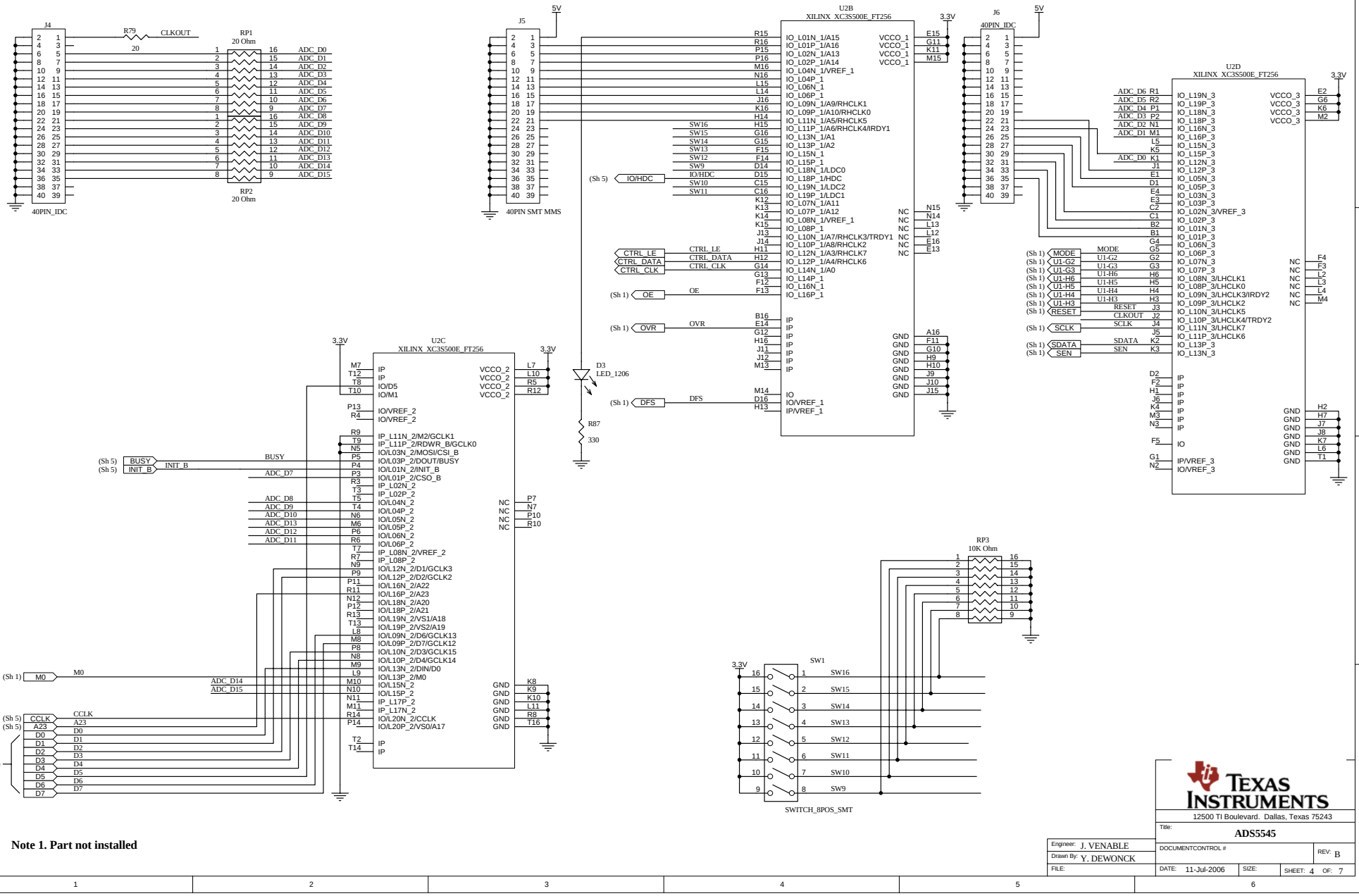
12500 TI Boulevard. Dallas, Texas 75243

Title:	ADS5545		
DOCUMENTCONTROL #		REV:	B
DATE: 11-Jul-2006	SIZE:	SHEET: 3	OF: 7


J4
40PIN_IDC
R79
20
CLKOUT
RP1
20 Ohm
RP2
20 Ohm
ADC_D0
ADC_D1
ADC_D2
ADC_D3
ADC_D4
ADC_D5
ADC_D6
ADC_D7
ADC_D8
ADC_D9
ADC_D10
ADC_D11
ADC_D12
ADC_D13
ADC_D14
ADC_D15
J5
40PIN SMT MMS
5V
U2B
XILINX_XC3S500E_FT256
3.3V
(Sh 5) IO/HDC
SW16
SW15
SW14
SW13
SW12
SW9
IO/HDC
SW10
SW11
CTRL_LE
CTRL_DATA
CTRL_CLK
(Sh 1) OE
(Sh 1) OVR
(Sh 1) DFS
D3
LED_1206
R87
330
J6
40PIN_IDC
U2D
XILINX_XC3S500E_FT256
(Sh 1) MODE
(Sh 1) U1-G2
(Sh 1) U1-G3
(Sh 1) U1-H6
(Sh 1) U1-H5
(Sh 1) U1-H4
(Sh 1) U1-H3
(Sh 1) RESET
(Sh 1) SCLK
(Sh 1) SDATA
(Sh 1) SEN
U2C
XILINX_XC3S500E_FT256
(Sh 5) BUSY
(Sh 5) INIT_B
(Sh 1) M0
(Sh 5) CCLK
(Sh 5) A23
(Sh 5) D0
(Sh 5) D1
(Sh 5) D2
(Sh 5) D3
(Sh 5) D4
(Sh 5) D5
(Sh 5) D6
(Sh 5) D7
RP3
10K Ohm
SW1
SW16
SW15
SW14
SW13
SW12
SW11
SW10
SW9
SWITCH_8POS_SMT
Note 1. Part not installed
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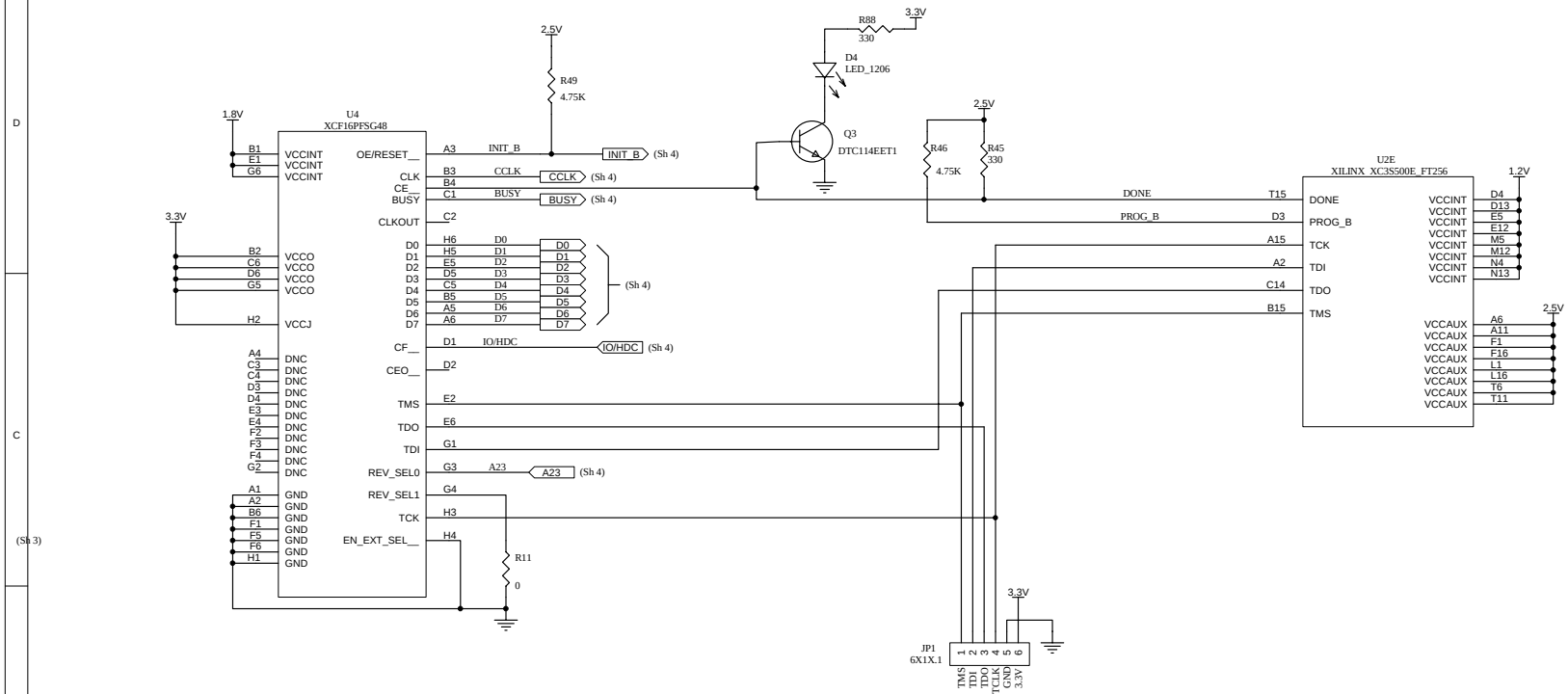
Title: ADS5545
DOCUMENTCONTROL #
REV: B
Engineer: J. VENABLE
Drawn By: Y. DEWONCK
FILE:
DATE: 11-Jul-2006
SIZE:
SHEET: 4 OF: 7



Note 1. Part not installed

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Drawn By:	Y. DEWONCK
FILE:	

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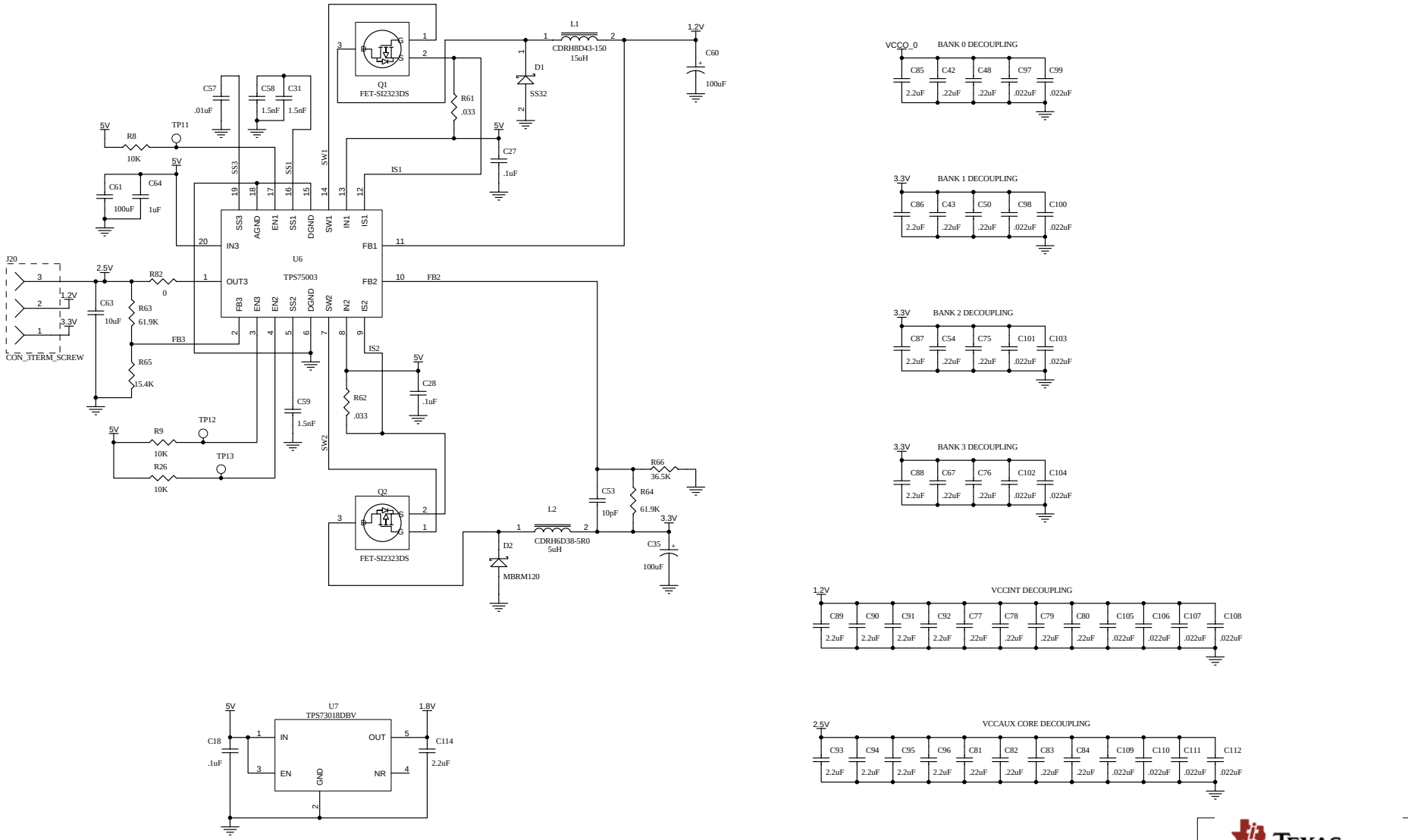
Title:	ADS5545		
DOCUMENTCONTROL #		REV:	B
DATE: 11-Jul-2006	SIZE:	SHEET: 5	OF: 7



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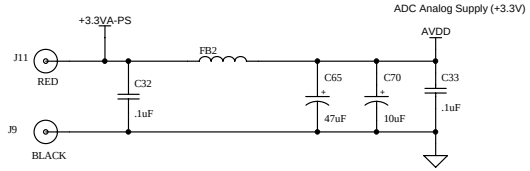
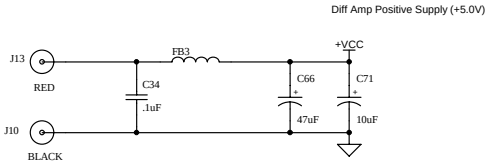
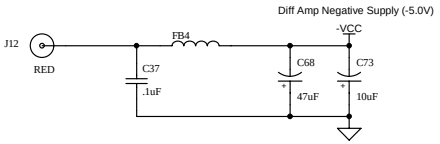
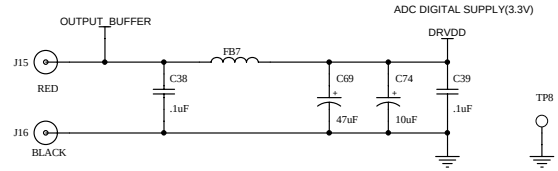
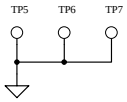
Engineer: J. VENABLE	Title: ADS5545		
Drawn By: Y. DEWONCK	SIZE:	DATE: 11-Jul-2006	REV: B
FILE:			SHEET: 6 OF: 7

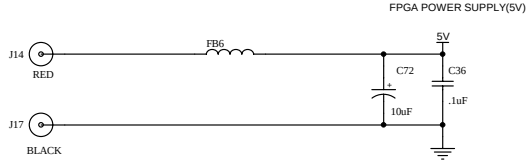


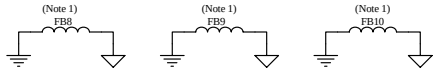












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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the AVDD voltage range of -0.3 V to 3.8 V and the DVDD voltage range of -0.3 V to 3.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265